What is claimed is :

1. An amplifier circuit comprising:

an amplification chain having at least an input stage and a differential output stage;

a common mode correction block acting on the input of the output stage as a function of a common mode voltage at the output of said stage and introducing a phase shift between its input and its output for frequencies close to the cut-off frequency of the circuit; and

in parallel with the correction block, a means introducing no phase shift between its input and its output and having at frequencies close to the circuit cut-off frequency an output impedance much smaller than the output impedance of the correction block.

2. The amplifier circuit of claim 1, wherein the output stage has a differential input and said means comprises a unity-gain stage receiving as an input the common mode voltage and having its output connected by two first identical capacitors to each of the inputs of the output stage.

3. The amplifier circuit of claim 2, wherein the stability of the amplification chain is ensured by two identical second capacitors, each arranged between one input and one output of the output stage; and wherein the first capacitors have a value such that they conduct, for frequencies close to the circuit cut-off frequency, a differential current smaller by one order of magnitude than the differential current crossing the second capacitors.

4. The amplifier circuit of claim 3, wherein the amplification chain further comprises an input stage with a differential input and output coupled to the input of the output stage and a feedback loop with a voltage divider coupling the output of the output stage to the input of the input stage.

5. The amplifier circuit of claim 2, wherein the unity-gain stage comprises a first MOS transistor of a first conductivity type connected as a source follower.

6. The amplifier circuit of claim 5, wherein the correction block comprises:

two second MOS transistors of a first conductivity type having sources connected to a ground via first resistors, the gate of one of the second transistors being connected between two second equal resistors series-connected between the output terminals of the output stage and the gate of the other one of the second transistors being connected to a reference voltage;

two third MOS transistors of a second conductivity type having drains connected to drains of the two second transistors, sources connected to a supply voltage and gates connected to the drain of that of the second transistors having its gate connected to the reference voltage;

two fourth transistors of the second conductivity type having sources connected to the supply voltage, gates connected to the drain of that of the second transistors having its gate connected between the second resistors, and drains forming the output terminals of the amplifier stage;

and wherein the first transistor is confounded with that of the second transistors having its gate connected between the second resistors.

7. The amplifier circuit of claim 5, wherein the correction block comprises:

two second MOS transistors of a first conductivity type having sources connected to a ground via first current sources, and connected together by a first resistor, the gate of one of the second transistors being connected between two second equal resistors series-connected between the output terminals of the output stage and the gate of the other one of the second transistors being connected to a reference voltage;

two third MOS transistors of a second conductivity type having drains connected to the drains of the two second transistors, sources connected to a supply voltage, and gates connected to the drain of that of the second transistors having its gate connected to the reference voltage;

two fourth transistors of the second conductivity type having sources connected to the supply voltage, gates connected to the drain of that of the second transistors having its gate connected between the second resistors, and drains forming the output terminals of the amplifier stage;

and wherein the first transistor is confounded with that of the second transistors having its gate connected between the second resistors.

8. The amplifier circuit of claim 6, wherein the output stage is formed of fifth and sixth MOS transistors of the second conductivity type having sources connected to the supply voltage, drains, forming the output terminals of the output stage, connected to second current sources, and gates forming the input terminals of the output stage, two Miller capacitors respectively connecting the gates of the fifth and sixth transistors to the drains of said transistors.

9. The amplifier circuit of claim 8, wherein the input stage comprises seventh and eighth (26B) MOS transistors of the first conductivity type having sources coupled to a third current source, drains forming the output terminals of the input stage and being respectively connected to the gates of the sixth and fifth transistors, and gates forming the input terminals of the input stage and being respectively connected by first impedances to the drains of the fifth and sixth transistors, and by second impedances to two input terminals of the circuit.

10. The amplifier circuit of claim 6, wherein the supply voltage is a positive voltage and the transistors of the first and second conductivity types are respectively N-channel and P-channel transistors.

11. A common mode correction circuit operable in a normal mode to develop a common mode feedback value on an output in response to an input signal applied on an input, and operable in a cut-off mode when the input signal is near a cut-off frequency to inhibit the development of the common mode feedback value on the output.

12. The common mode correction circuit of claim 11 wherein the correction circuit includes a cut-off circuit coupled between the input and output of the correction circuit, and wherein the cut-off circuit is operable to provide a cut-off output impedance in parallel with an output impedance of the correction circuit when the input signal is near the cut-off frequency, the cut-off output impedance being much smaller than the output impedance of the correction circuit near the cut-off frequency.

13. The common mode correction circuit of claim 12 wherein the correction circuit includes differential inputs and differential outputs, and wherein the cut-off circuit is

operable to provide respective cut-off output impedances in parallel with each of the differential outputs.

14. The common mode correction circuit of claim 12 wherein the cut-off circuit introduces an approximately unity gain and a substantially zero phase shift between signals developed on outputs coupled to the outputs of the correction circuit and signal applied on inputs coupled to the inputs of the correction circuit near the cut-off frequency.

15. An amplifier circuit, comprising:

a first differential amplifier having at least one input and differential outputs;

a common mode correction circuit having inputs coupled to the outputs of the first differential amplifier and having an output coupled to the input of the first differential amplifier, the common mode correction circuit operable in a normal mode to develop a common mode feedback value on its output in response to signals applied on its inputs, and operable in a cut-off mode when the input signals are near a cut-off frequency to inhibit the development of the common mode feedback value on the output.

16. The amplifier circuit of claim 15 wherein the first differential amplifier includes differential inputs and further includes Miller capacitors coupled between each input and output, and wherein the cut-off capacitors have values that are sufficiently less than values of the Miller capacitors such that a differential current flowing through the cut-off capacitors is approximately an order of magnitude less than a differential current flowing through the Miller capacitors.

17. The amplifier circuit of claim 16 wherein the correction circuit includes a cut-off circuit coupled between the inputs and outputs of the correction circuit, and wherein the cut-off circuit is operable to provide cut-off output impedances in parallel with output impedances of the correction circuit when the signals at the output of the first differential amplifier are near the cut-off frequency, the cut-off output impedances being much smaller than the output impedances of the correction circuit near the cut-off frequency.

18. The amplifier circuit of claim 17 wherein the cut-off impedances have values that are approximately one fifth the values of the Miller capacitances.

19. The amplifier circuit of claim 18 further comprising a second differential amplifier having inputs adapted to receive input signals and having outputs coupled to the inputs of the first differential amplifier.

20. The amplifier circuit of claim 19 wherein the cut-off circuit introduces an approximately unity gain and a substantially zero phase shift between signals developed on outputs coupled to the outputs of the correction circuit and signal applied on inputs coupled to the inputs of the correction circuit near the cut-off frequency.

21. An electronic system, comprising:

electronic circuitry including an amplifier circuit, including,

a first differential amplifier having at least one input and differential outputs;

a common mode correction circuit having inputs coupled to the outputs of the first differential amplifier and having an output coupled to the input of the first differential amplifier, the common mode correction circuit operable in a normal mode to develop a common mode feedback value on its output in response to signals applied on its inputs, and operable in a cut-off mode when the input signals are near a cut-off frequency to inhibit the development of the common mode feedback value on the output.

22. The electronic system of claim 21 wherein the electronic circuitry comprises a variable gain amplifier circuit.

23. The electronic system of claim 22 wherein the variable gain amplifier circuit comprises an operational amplifier circuit.

24. A method of controlling a common mode feedback value in an amplifier having at least one input and differential outputs, the method comprising:

developing a feedback value responsive to signals on the outputs of the amplifier when the frequency of an input signal applied to the differential amplifier is not near a cut-off frequency;

applying the feedback value to the input of the differential amplifier; and

disabling application of the feedback value to the input of the amplifier when the frequency of the input signal is near the cut-off frequency.

25. The method of claim 24 wherein disabling application of the feedback value to the input of the amplifier when the frequency of the input signal is near the cut-off frequency comprises coupling an impedance in parallel with the input of the differential amplifier, the impedance having a sufficiently small value to reduce the value of the feedback value applied to the input of the amplifier and thereby effectively disable application of the feedback value to the input of the amplifier.

26. The method of claim 25 wherein the impedance has a value that is a function of the values of Miller capacitances coupled between the input and outputs of the differential amplifier.